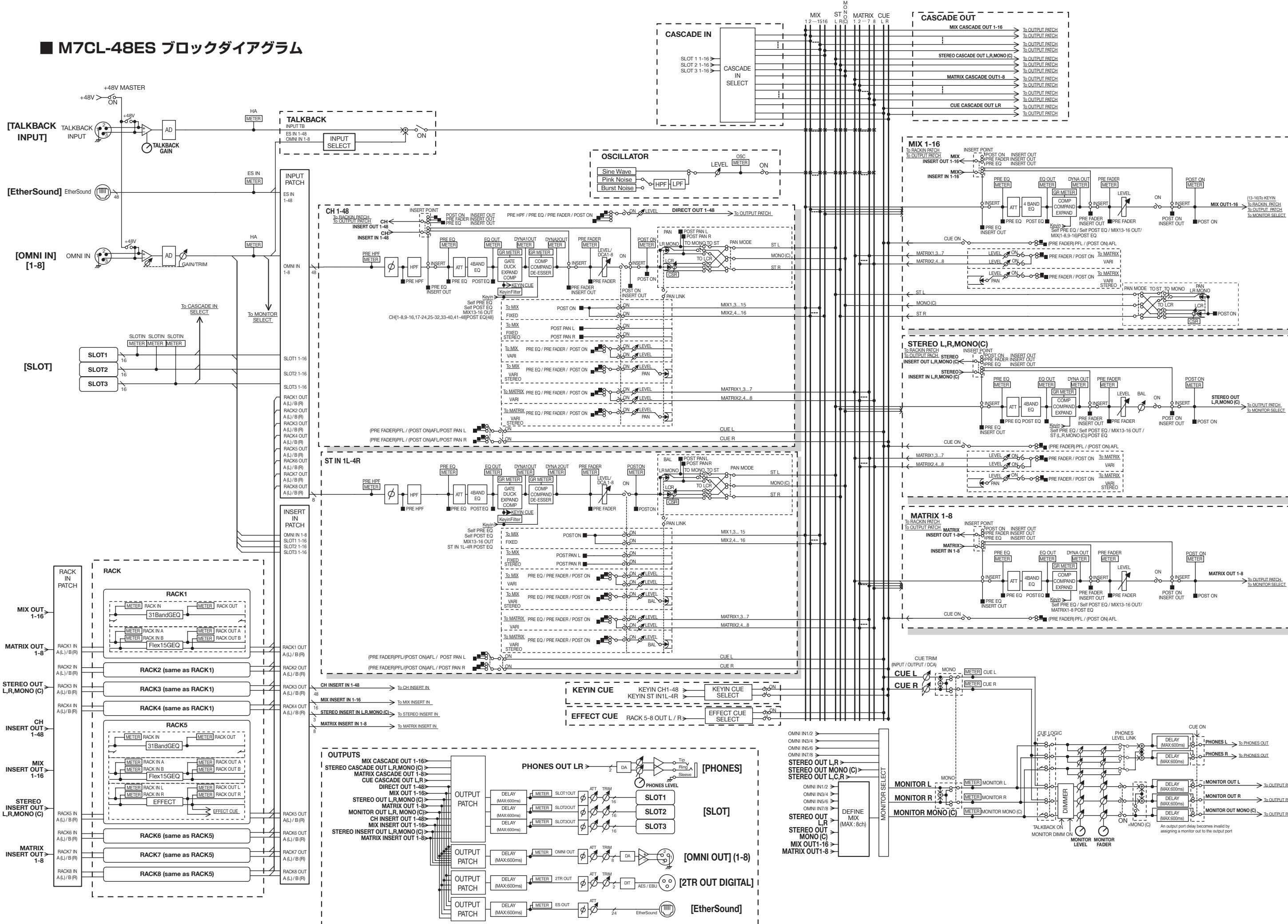


M7CL-48ES ブロックダイアグラム



An output port delay becomes invalid by assigning a monitor out to the output port